UNITED STATES DISTRICT COURT
SOUTHERN DISTRICT OF NEW YORK

FIFTH GENERATION COMPUTER CORPORATION,

Plaintiff,

-v-

INTERNATIONAL BUSINESS MACHINES CORPORATION,

Defendant.

09 Civ. 2439 (JSR)

ORDER

JED S. RAKOFF, U.S.D.J.

In this action, plaintiff Fifth Generation Computer Corporation, the current owner of U.S. Patents 4,860,201 ("the '201 patent") and 6,000,024 ("the '024 patent") alleges that defendant International Business Machines Corporation infringed one or both of those patents. Following briefing, the Court, on August 24, 2004, held a one-day "Markman" hearing to address those terms of the patents whose construction is disputed. See Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996).

After full consideration, the Court construes the disputed terms as follows:

(A) With respect to the '201 patent:

1. "binary tree" means an arrangement of nodes where each node has a single parent and two children nodes, except the root node, which has no parent, and the leaf nodes, which have no children.

2. "subtree" means a subset of the binary tree such that each node has a single parent and two children nodes, except

the root node, which has no parent, and the leaf nodes, which have no children.

3. "without direct control of the processors of the processing elements" means the function is performed independently by the I/O device without receiving instructions from its associated processor.

4. "each in a time on the order of the logarithm of the number of processing elements in said binary tree or subtree multiplied by the time for the broadcasting of information from a parent processing element to child processing elements connected thereto, and the time required to determine priority among values of information received from the processor of a processing element and the child processing elements connected thereto, respectively" means the broadcasting operation is capable of being performed in one clock cycle, multiplied by the base 2 algorithm of the number of processing elements in the binary tree; and the priority is capable of being determined in two clock cycles, multiplied by the base 2 logarithm of the number of processing elements in the binary tree.

5. "single instruction multiple data mode" means a mode where each processing element is first loaded with its own data and then a single stream of instructions is broadcast to every processing element in the binary tree.

6. "multiple instruction multiple data mode" means a mode where each processing element is first loaded with its local program and data and then each processing element is logically disconnected from its neighbor processing element and executes independently.

(B) With respect to the '024 patent:

1. "binary tree computer system" means a computer system of nodes connected in a binary tree configuration.

2. "binary tree configuration" means an arrangement of nodes where each node has a single parent and two children nodes, except the root node, which has no parent, and the leaf nodes, which have no children.

3. "host computer" means a computer that is connected to and controls the binary tree of bus controllers.

4. "bus controllers" means controllers that transfer instructions and data from the host computer to the connected processing elements and data from the connected processing elements to the host computer over a bus.

5. "root bus controller" means the bus controller at the highest order position of the binary tree computer system that connects the binary tree to the host computer and which has no parent bus controller.

An opinion giving the reasons for these ruling will issue in due course.

SO ORDERED.

JED S. RAKOFF, U.S.D.J.

Dated: New York, New York
August 31, 2009